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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,882	HALL ET AL.	
	Examiner	Art Unit	
	Andrew Lai	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3-6,8,9,11 and 12,14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Fechalos (US 4,737,950).

Fechalos discloses "a network interface LSI for use in an improved switching system", col. 1 lines 6-7, using plurality of "concentrators" (fig. 1a, items 10), comprising the following features:

- **With respect to independent claims 1 and 12**

Regarding claim 1, *an apparatus* (fig. 1 "concentrator 10" of which fig. 2 shows therein "a general block diagram of the primary modules", col. 2 lines 52-53) *for fixing latency of an operation within a deterministic region* (fig. 2 depicting the whole *deterministic region* of the concentrator, noting that the region is connected with "primary/secondary" buses 30/32, which is well known in the art to provide *fixing* or *fixed latency*) *on a network* (fig. 2 "to/from host system" corresponding to fig. 1 "host switching system 12"), *the apparatus comprising:*

a network interface modem (fig. 2 "T1 interface 36") *in communication with the network* (fig. 2 depicting "T1 interface 36" sending/receiving data "to/from host system");

a high priority module (fig. 2, a hardware control subsystem, "HWSS" hereinafter, comprised of "CPU 26", "BIF 40", "I/O 42", "DISC 44", "PAD 46", etc.) *in communication with the network interface* (fig. 2 depicting said "HWSS" *in communication with* said "T1 interface" via "primary/secondary bus 30/32");

the high priority module ("HWSS") *comprising a packet assembler/disassembler* (fig. 2 "PAD 46", or "packet assembler/disassembler (PAD) 46", col. 5 line 54), *and hardware* (fig. 2, e.g., "CPU 26", "I/O 42", etc.) *for performing at least one operation* (figs. 4 and 5, where fig. 4 "illustrating the levels of operation in the concentrator", col. 2 lines 56-57, and fig. 5 "illustrating the functional operations of the different levels of the fig. 4 diagram", col. 2 lines 58-59, wherein listed operations including, e.g., at "level 1" "network time slot assignment", "general call processing", etc., at "level 2", "data formatting", "packet assembly", etc., and, at "level 3", "encoded signaling translation", etc.); *and*

at least one deterministic peripheral device (Fechalos discloses various such devices, of which one unique example is fig. 2 "CLK 48", or "clock generator 48", col. 5 line 55, and additionally others, such as "when equipped, the I/O module 42 provides interface between external peripheral devices", col. 5 lines 58-60) *connected to the high priority module* (fig. 2 depicting the connection of said "CLK 48" with the "HWSS" and fig. 1 depicting various other *peripheral devices*, such as "analog and digital subscriber terminal equipment 14", col. 3 lines 31-32, "key telephone subscribers 20", col. 4 lines 14-15, "remote subscribers 22", col. 4 lines 58-59, and even "local area networks (LAN) 24", col. 5 line 16);

wherein the fixed latency hardware ("HWSS") *performs operations on the deterministic peripheral device* (refer to figs. 4 and 5, wherein fig. 4 indicating "level 1" operations by "CPU 26", which operations include, as fig. 5 shows, "General Call Processing" for data calls for, e.g. the "digital subscriber terminal equipment 14" and/or "Key Telephone Subscribers 20" as cited above) *according to instructions* ("routing information", col. 8 line 62) *received and interpreted by the packet assembler/disassembler* (refer to fig. 4 and see "the packet assembler/disassember (PAD) 46 generates routing information requests to the CPU 26 for each data call", col. 8 lines 61-63, noting that such "generates routing information" requires the *packet assembler/disassembler receive and interpret* data packets).

Regarding claim 12, *a method of performing an operation* ("a novel network interface LSI device for use with switching systems", col. 1 lines 42-43, which "switching" is well known in the art as *an operation* associated with certain type of *method* or algorithm) *within a deterministic region* (fig. 2 depicting a whole *region* of a "concentrator 10" shown in fig. 1, which forms the core of said "LSI", noting that various elements in the region are interconnected using "primary/secondary" buses 30/32, which buses are well known in the art to provide *a deterministic* configuration) *comprising:*

proving a high priority module (fig. 2, a hardware control subsystem, "HWSS" hereinafter, comprised of "CPU 26", "BIF 40", "I/O 42", "DISC 44", "PAD 46", etc.) *connected to a network interface modem* (fig. 2 showing "T1 interface 36" and depicting said "HWSS" *connected to* the "T1 interface" via "primary/secondary bus 30/32") *in*

communication with a network (fig. 2 depicting "T1 interface 36" sending/receiving data "to/from host system" corresponding to fig. 1 "host switching system 12");

recognizing by the high priority module a packet as the operation (fig. 2 showing, within the "HWSS", a "PAD 46" or "packet assembler/disassembler (PAD) 46", col. 5 line 54, which "generates routing information requests to the CPU 26 for each data call", col. 8 lines 61-63, and said "CPU 26" performs a "level 1" operations, fig. 4, including "General Call Processing", fig. 5, noting it is well known in the art that "general call processing" has to rely on "routing information"); *and*

performing the operation within the deterministic region ("general call processing" have to be processed via the various elements of the "HWSS", such as, for example, fig. 2 "I/O 42" which "provides interface between external peripheral devices", col. 5 line 59-60) *and on a peripheral device* ("when equipped, the I/O module 42 provides interface between external peripheral devices", col. 5 lines 58-60, of which one unique example is fig. 2 "CLK 48", or "clock generator 48", col. 5 line 55, and fig. 1 also shows various other types, such as "analog and digital subscriber terminal equipment 14", col. 3 lines 31-32, "key telephone subscribers 20", col. 4 lines 14-15, "remote subscribers 22", col. 4 lines 58-59, and even "local area networks (LAN) 24", col. 5 line 16);

- **With respect to associated dependent claims**

  Claims depending from claim 1:

  Regarding claim 3, *wherein the hardware* (see, e.g., fig. 2 "CPU 26" and "BIF 40") *of the high priority module* ("HWSS") *is selected from the group consisting of at*

least one hardwired circuit, at least one integrated circuit, and at least one FPGA (fig. 2 depicting *hardwired* "primary bus" 30 linking said CPU and BIF).

Regarding claim 4, *wherein the packet assembler/disassemebler comprises* (fig. 2 "PAD 46") *a packet assembler and a packet disassembler wherein the packet assembler and the packet disassembler are two separate circuits* (it is well known in the art that a "PAD" in a packet communication device has to have *two separate circuits* in it, one dealing with outgoing packet assembling and the other with incoming disassembling).

Regarding claim 5, *wherein the at least one deterministic peripheral device is selected from the group consisting of a clock* (fig. 2 "CLK 48" as a "clock generator" which itself must have clocking function), *a local clock source* (again "clock generator 48"), *at least one timer* ("CLK 48" is also a timer), *at least one analog circuit, at least one digital circuit* (fig. 1 "both analog and digital subscriber terminal equipment 14", col. 3 lines 31-32), *and at least one actuator.*

Regarding claim 6, *wherein the clock is a hardware integrated circuit* (fig. 2 "CLK 48" in a single block suggesting *a hardware integrated circuit*).

Regarding claim 8, *wherein the clock is synchronized to a GPS or a clock source over a LAN* ("a clock means for receiving a predetermined fixed external clock signal and a reset signal for synchronization", col. 2 lines 19-21).

Regarding claim 9, *wherein the high priority module* ("HWSS") *is in communication with devices selected from the group consisting of a data buffer, at least one router, at least one node, at least one tool port, at least one data acquisition device*

(refer to fig. 2 and see "when equipped, the I/O module 42 provides interface between external peripheral devices, such as CRT's, printers, modems, and tape units", col. 5 lines 58-61).

Regarding claim 11, *wherein the deterministic region* (fig. 2 showing said region) *encompasses devices selected from the group consisting of the high priority module* ("HWSS"), *the network interface modem* ("T1 interface 36") *and the at least one deterministic peripheral device* ("CLK 48").

Claims depending from Claim 12: **Regarding claim 17**, *wherein the method further comprises the step of forwarding a packet by the high priority module*

Regarding claim 14, *wherein the high priority module* (e.g. "CPU 26" in fig. 2) *fills a field in the packet with data from the peripheral device* (e.g. "digital subscriber terminal equipment 14" of fig. 1, and see fig. 11a depicting an example wherein said "CPU" "Recv. RFS + ID. Find idle TS [time slot]. Format ID, TS, Connect message for BIF", noting the "RFS" originally comes from "interface" "user ports", shown also in fig. 11a, and said "format ID, TS" will have to perform relevant *filling a field in the packet with data from the peripheral deive*).

Regarding claim 15, *wherein the high priority module* ("HWSS") *connected to a buffer* ("The CPU 26 communicates to the primary bus 30", col. 8 lines 41-42, and "providing each primary bus with a 128 byte buffer", col. 8 lines 46-47).

Regarding claim 16, *wherein the packet is received from a device selected from the group consisting of a network interface modem, a buffer, a router, a local node, a tool port, and a data acquisition device.*

Regarding claim 17, *wherein the method further comprises the step of forwarding a packet by the high priority module.*

Regarding claim 18, *wherein the packet is forwarded to a device selected from the group consisting of a network interface modem, a buffer, a router, a local node, a tool port, and a data acquisition device.*

(fig. 1 depicting multiple concentrators 10 communicating with each other via "host switching system 12" using "T1" connections. Therefore, such communications inevitably result in, regarding claim 16, that *packet is received from network interface modem*, which is the "T1 interface" shown in fig. 2, and regarding claim 17, *forwarding packets by the high priority module*, and further regarding claim 18, *forwarded to a network interface modem* such as the "T1 interface").

Regarding claim 19, *wherein the packet forwarded is selected from the group consisting of the packet and a packet modified by the operation* (fig. 11a depicting "CPU" "Recv. RFS + ID. Find idle TS [time slot]. Format ID, TS, Connect message for BIF", which "format ID, TS" will have to involve *a packet* being *modified by the operation*).

Regarding claim 20, *wherein the operation is a high priority operation which is performed immediately upon recognition* ("provide fast response to data call request", col. 8 line 66).

3. Claims 21-25,29,30 are rejected under 35 U.S.C. 102(b) as being anticipated by Tubel et al (US 5,959,547, Tubel et al hereinafter).

Tubel discloses "well control systems employing dowhole network" (col. 1 lines 1-2 and see fig. 2 for "downhole network") using a plurality of "downhole tools and other production equipments" (col. 4 lines 18-19) comprising the following features:

Regarding claim 21, *an apparatus for fixing latency of an operation within a deterministic region* ("apparatus for the control of oil and gas production wells", col. 1 lines 19-20, for which operators "use handheld terminal to also set the time delay for the tools to turn itself on", col. 11 lines 16-17) *on a downhole network integrated into a tool string* (fig. 2 depicting "downhole network" using a plurality "downhole control system 22", col. 16 line 67, which "control system" being *integrated into tool strings* comprised of, e.g. "packer 71", col. 17 line 5, "sliding sleeve 79 and perforating tools 81", col. 17 lines 8-9); *the apparatus comprising:*

a control device near the surface of the downhole tool string (fig. 1 "surface control system 24", col. 9 lines 28-29), *the control device* (fig. 5 "depicting a surface control system", col. 7 lines 26-27) *comprises a network interface modem in communication with the downhole network* (fig. 5 "surface to borehole transceiver 34"), *a high priority communication module* (fig. 5 "data acquisition & pre-processing 42" and "computer control 30") *in communication with the network interface modem* (fig. 5 depicting bi-directional communication between "data acquisition & pre-processing 42" and "surface to borehole transceiver 34"), *and at least one deterministic peripheral device* (fig. 5, e.g. "printer plotter 40" or "depth measurement system 44") *connected to the high priority module* (fig. 5 depicting "printer plotter 40" or "depth measurement system 44" connected to "computer control 30");

a downhole device (fig. 6 "depicting a downhole production well control system", col. 7 lines 36-37, as a detailed view of fig. 2 "downhole control system 22") *comprising a netowrk interface modem in communication with the downhole network* (fig. 6 "downhole to surface transceiver system 52" sending/receiving data "to/from surface"), *a high priority module* (fig. 6 "processor based data processing and control system 50") *in communication with the network interface module* (fig. 6 depicting bi-directional communication between "downhole to surface transceiver system 52" and "processor based data processing and control system 50"), *and at least one deterministic peripheral device* (fig. 6, e.g. "electro mechanical drivers 60" or "other electronic control apparatus 62") *connected to the high priority module* (fig. 6 depicting the connection of "electro mechanical drivers 60" or "other electronic control apparatus 62" with "processor based data processing and control system 50")

Regarding claim 22, *wherein the control device* ("surface control system 24") *is a computer* (refer to fig. 5 and see "the surface system 24 is composed of a computer system 30", col. 9 line 48).

Regarding claim 23, *wherein the network interface modem* ("surface to borehole transceiver 34") *and the high priority module* ("data acquisition & pre-processing 42" and "computer control 30") *are on an insertable computer card* ("computer system 30 may be comprised of a personal computer or a work station with a processor board", col. 9 lines 50-52).

Regarding claim 24, *wherein the control device* ("surface control system 24") *further comprise a connection to a local area network* (fig. 1 depicting "surface control

system 24" having wireless *connections to a local area network* comprised of various "surface control systems 24" and "a remote central control center 10", col. 8 line 42).

Regarding claim 25, *wherein the at least one deterministic peripheral device is selected from the group consisting of a local clock source, at least one analog circuit, at least one actuator, a lock and a hardware clock integrated circuit* (figs. 5A and 5B, as "a preferred system [part of fig. 5] for sensing downhole pressure condition", col. 10 lines 42-43, showing a "EPLD 304" which is "comprised of six counters", col. 10 lines 57-58, one of which is "pulse counter", fig. 5B, which further has "the clock in the pulse counter", col. 11 line 4. Therefore, the entire structure suggests *a clock* or *a hardware clock integrated circuit*).

Regarding claim 29, *wherein the deterministic region* (fig. 5) *encompasses devices on the network* (all modules in fig. 5 are *on the* downhole network) *selected from the group consisting of transmission media* ("the downhole network consists of an interconnecting cable", col. 22 lines 49-50), *the high priority module* (fig. 5, e.g. "computer control 30), *the network interface modem* (fig. 5 "surface to borehole transceiver 34"), *and the at least one deterministic peripheral device* (fig. 5, e.g., "printer plotter 40").

Regarding claim 30, *wherein the downhole device* ("downhole control system") *comprises non-deterministic devices selected from the group consisting of a data buffer* (fig. 6 "recorder 66A"), *at least one router, at least one node, local node circuitry, at least one tool port* (fig. 6 "electro mechanical drivers 60") *and at least one data acquisition device* (fig. 6 "data acquisition system 54")

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fechalos (US 4,737,950).

Fechalos discloses claimed limitation in paragraph 2 above as applied to claim 1, including, **regarding claim 10**, *the high priority module* ("HWSS" cited for claim 1) and *the network interface modem* ("T1 interface") as shown in Fechalos fig. 2.

Even though Fechalos does not disclose, in context of fig. 2, that *the high priority module is part of the network interface modem*, as recited in claim 10, Fechalos however disclose that the whole circuit of fig. 2 showing "the primary modules in the concentrator" is in fact "the network interface LSI" (col. 1 lines 66-67, which is shown in fig. 1 as "concentrator 10" interfacing the "host switching system 12" with a plurality of peripheral devices 14, 20, 22 and 24). Therefore, it would have been obvious to one of ordinary skill to modify the configuration of fig. 2 of Fechalos, as merely a design alternative, by incorporating the same concept taught by Fechalos himself of integrating the HWSS into the interface, which may provide a more confined network interface unit for space saving purposes and/or possibly faster processing because signals

transmitted among various modules may travel a shorter distance than on the buses provided in fig. 2.

6. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fechalos (US 4,737,950) in view of Tubel et al (US 5,959,547, Tubel hereinafter).

Fechalos discloses claimed limitations in paragraph 2 above as applied to claims 1 and 12.

Tubel discloses "a plurality of downhole control systems interconnected by a network" (Abstract lines 1-2).

Fechalos does not but Tubel does disclose:

Regarding claims 2, *wherein the network is integrated into a downhole network.*

Regarding claim 13, *wherein the network is integrated into a downhole tool string.*

(see Tubel's fig. 11, which is "a diagrammatic view of an exemplary application of the downhole network", col. 22 lines 32-33, and "the downhole network consists of an interconnecting cable that supplies surface power and facilitates communications", col. 22 lines 49-50, through which cable "the downhole control systems communicate directly with each other transferring information and commands as necessary", Abstract lines 4-6, wherein the "downhole control systems" comprise "as an alternative to downhole sensors, wire line production logging tools are also used to provide downhole data", col. 2 lines 49-51).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of Fechalos by adding the downwhole network system

of Tubel to the host switching system of Fechalos in order to provide an "automatic control" (Tubel, col. 4 line 58) over for a well "for automatically controlling downhole tools in response to sensed selected downhole parameters" (Tubel, col. 4 lines 55-57).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fechalos (US 4,737,950) in view of Jain et al (US 5,959,547, Tubel hereinafter).

Fechalos discloses claimed limitations in paragraph 2 above as applied to claim 5 including *the local clock source* (fig. 2 "CLK 48" or "clock generator 48").

Jain discloses an invention wherein "a telecommunications network being operable as a packet switch and as a circuit switch" (Abstract lines 1-2) using plurality of "bus controllers" (fig. 1) each having an internal "clock generator" (fig. 2 "clock generator 205").

Fechalos does not but Jain does disclose *wherein the local clock source* ("clock generator") *is selected from the group consisting of at least one crystal, at least one transistor, at least one oscillator, at lease on RC circuit, at least one LC circuit, and at least one RLC circuit* (Jain's fig. 2 "clock gen. 205" and see "the clock generator in one example consists of an internal crystal oscillator", col. 5 lines 54-56).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the clock generator of Fechalos by incorporating the clock crystal oscillator of Jain into Fechalos in order to provide an accurate timing mechanism that "accommodates communication of digital signals of asynchronous and synchronous natures respectively" (Jain, col. 1 lines 11-13).

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tubel et al (US 5,959,547, Tubel hereinafter) in view of Jain et al (US 4,608,685, Jain hereinafter).

Tubel discloses claimed limitations in paragraph 3 above as applied to claim 25 including *the local clock source* ("the clock in the pulse counter").

Jain discloses an invention wherein "a telecommunications network being operable as a packet switch and as a circuit switch" (Abstract lines 1-2) using plurality of "bus controllers" (fig. 1) each having an internal "clock generator" (fig. 2 "clock generator 205").

Tubel does not but Jain does disclose *wherein the local clock source* ("clock generator") *is selected from the group consisting of at least one crystal, at least one transistor, at least one oscillator, at lease on RC circuit, at least one LC circuit, and at least one RLC circuit* (Jain's fig. 2 "clock gen. 205" and see "the clock generator in one example consists of an internal crystal oscillator", col. 5 lines 54-56).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the clock in the pulse counter of Tubel by incorporating the clock crystal oscillator of Jain into Tubel in order to provide an accurate timing mechanism that "accommodates communication of digital signals of asynchronous and synchronous natures respectively" (Jain, col. 1 lines 11-13).

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tubel et al (US 5,959,547, Tubel hereinafter) in view of LoGalbo et al (US 5,220,676, LoGalbo hereinafter).

Tubel discloses claimed limitation in paragraph 3 above as applied to claim 25. Tubel further discloses *the clock is synchronized* ("provide the synchronization between the devices that are attempting to setup communications link", col. 21 lines 64-65, noting that such "synchronization between the devices" actually means synchronization of the *clocks* therein).

Tubel however does not disclose regarding claim 27 synchronization *to a GPS clock.*

LoGalbo discloses "an improved synchronization method and apparatus" (Abstract line 1) for "remote sites in an absolute time simulcast system" (col. 1 lines 7-8) comprising **regarding claim 27** *the clock is synchronized to a GPS clock* (refer to fig. 4 and see "one method of synchronizing the remotes 421, 431 together and to the prime 403 is to have a remote synchronization clock which is derived from a signal 415 received from a GPS satellite 401", col. 2 lines 58-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the downhole network system of Tubel by adding the GPS synchronization method of LoGalbo to Tubel in order to provide precise mechanism "for synchronization that will achieve [better] signal timing shown in [LoGablbo's] fig. 3" (LoGalbo col. 1 lines 62-63) wherein "the corresponding sinusoidal signals are correctly aligned with respect to time and phase" (col. 2 lines 3-5), which is especially important

for, for example, oil industrial application involving time precise operations of downwhole tools.

10. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tubel et al (US 5,959,547, Tubel hereinafter) in view of Fechalos (US 4,737,950).

Tubel discloses claimed limitations in paragraph 3 above as applied to claim 25 including *the high priority module* (fig. 5, e.g. "computer control 30") and *the network interface modem* (fig. 5 "surface to borehole transceiver 34").

Tubel however does not expressly disclose, regarding claim 28, said "computer control 30" *is part of the* "surface to borehole transceiver 34").

Fechalos discloses "a network interface LSI for use in an improved switching system", col. 1 lines 6-7, which "network interface LSI" is in the form of "concentrator" (fig. 1a depicting "concentrator 10" interfacing "host switching system 12" with various peripheral devices 14, 20, 22 and 24), comprising **regarding claim 28**, *wherein the high priority module* (fig. 2, e.g. "CPU 26") *is part of the network interface modem* (the "concentrator 10").

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the control systems of Tubel by incorporating the interface configuration of Fechalos into Tubel in order to provide a more robust and user friendly system "which can function in a switching system capable of assuming different personalities depending o the application" (Fechalos, col. 1 lines 33-36).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,157,392 provides telemetry network for downhole multistation sersmic recording tools.

US 4,901,289 discloses a system for acquiring and recording signals delivered by a set of sensors disposed in one or more probes lowered into a well.

US 2002/0120800 discloses a method for processing a remote interrupt signal or a remote event.

US 7,085,237 provides method and apparatus for routing alarms in a signaling server for daisy-chain type of networks.

US 6,895,189 teaches a synchronization system using GPS receiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Lai whose telephone number is 571-272-9741. The examiner can normally be reached on M-F 7:30-5:00 EST, Off alternative Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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